

# **JEDEC STANDARD**

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## **Ball Grid Array Pinouts Standardized for 32-Bit Logic Functions**

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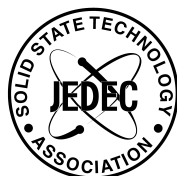
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**BALL GRID ARRAY PINOUTS STANDARDIZED FOR 32-BIT LOGIC FUNCTIONS**

(Formerly JEDEC Board Ballot JCB-99-51, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

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**1 Background**

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**1.1 Purpose**

To provide a pinout standard for dual-die 32-bit logic devices offered in a 96- and 114-ball grid array package for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

**1.2 Scope**

This standard defines device pinout for 32-bit wide buffer, driver and transceiver functions. This pinout specifically applies to the conversion of DIP-packaged 16-bit logic devices to LFBGA-packaged dual-die 32-bit logic devices.

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**2 Definitions for the purpose of this document**

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**2.1 Definitions**

DIP: Dual In-line Pin Package (gull-wing)

LFBGA: Low-Profile Fine-Pitch Ball Grid Array (MO-205)

SSOP: Shrink Small-Outline Package; 0.25" lead pitch; 0.3" wide body (MO-118)

TSSOP: Thin Shrink Small-Outline Package; 0.5-mm lead pitch; 6.4-mm wide body (MO-153)

TVSOP: Thin Very Small-Outline Package; 0.4-mm lead pitch; 4.4-mm wide body (MO-194)

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**3 Pinout standard**

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**3.1 Description**

The following criteria shall be used to convert existing 16-bit logic device functions offered in 48- and 56-pin DIP packages (SSOP, TSSOP, TVSOP) to 32-bit logic device functions offered in 96- and 114-ball LFBGA packages:

A. Attributes for the LFBGA packages shall be as follows:

- (1) 96-Ball, 0.8-mm ball pitch with 5.5-mm  $\times$  13.5-mm body size and 6-row  $\times$  16-column ball matrix, or the
- (2) 114-Ball, 0.8-mm ball pitch with 5.5-mm  $\times$  16.0-mm body size and 6-row  $\times$  19-column ball matrix.

B. Device conversion shall be as follows:

DIP package	LFBGA package
48-pin	96-ball
56-pin	114-ball

C. The pinout conversions shall be in accordance with the diagrams shown in section 3.3 and 3.6.

3.2 96-ball LFBGA (MO-205CC)

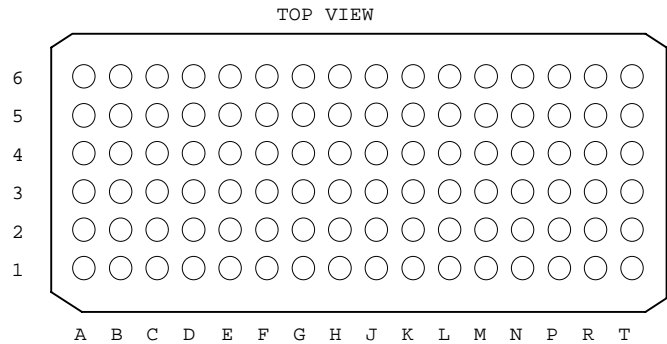


Figure 1. Pinout configuration

3.3 Pin conversion for 96-ball LFBGA

The pin conversion adopts the naming convention of logic devices in 48-pin packages (e.g. SSOP, TSSOP, TVSOP).

6	A46 <sup>¶</sup>	A43 <sup>¶</sup>	A40 <sup>¶</sup>	A37 <sup>¶</sup>	A35 <sup>¶</sup>	A32 <sup>¶</sup>	A29 <sup>¶</sup>	A27 <sup>¶</sup>	B46 <sup>¶</sup>	B43 <sup>¶</sup>	B40 <sup>¶</sup>	B37 <sup>¶</sup>	B35 <sup>¶</sup>	B32 <sup>¶</sup>	B29 <sup>¶</sup>	B27 <sup>¶</sup>
5	A47 <sup>¶</sup>	A44 <sup>¶</sup>	A41 <sup>¶</sup>	A38 <sup>¶</sup>	A36 <sup>¶</sup>	A33 <sup>¶</sup>	A30 <sup>¶</sup>	A26 <sup>¶</sup>	B47 <sup>¶</sup>	B44 <sup>¶</sup>	B41 <sup>¶</sup>	B38 <sup>¶</sup>	B36 <sup>¶</sup>	B33 <sup>¶</sup>	B30 <sup>¶</sup>	B26 <sup>¶</sup>
4	A48 <sup>§</sup>	A45 <sup>†</sup>	A42 <sup>‡</sup>	A39 <sup>†</sup>	A34 <sup>†</sup>	A31 <sup>‡</sup>	A28 <sup>†</sup>	A25 <sup>§</sup>	B48 <sup>§</sup>	B45 <sup>†</sup>	B42 <sup>‡</sup>	B39 <sup>†</sup>	B34 <sup>†</sup>	B31 <sup>‡</sup>	B28 <sup>†</sup>	B25 <sup>§</sup>
3	A1 <sup>§</sup>	A4 <sup>†</sup>	A7 <sup>‡</sup>	A10 <sup>†</sup>	A15 <sup>†</sup>	A18 <sup>‡</sup>	A21 <sup>†</sup>	A24 <sup>§</sup>	B1 <sup>§</sup>	B4 <sup>†</sup>	B7 <sup>‡</sup>	B10 <sup>†</sup>	B15 <sup>†</sup>	B18 <sup>‡</sup>	B21 <sup>†</sup>	B24 <sup>§</sup>
2	A2 <sup>¶</sup>	A5 <sup>¶</sup>	A8 <sup>¶</sup>	A11 <sup>¶</sup>	A13 <sup>¶</sup>	A16 <sup>¶</sup>	A19 <sup>¶</sup>	A23 <sup>¶</sup>	B2 <sup>¶</sup>	B5 <sup>¶</sup>	B8 <sup>¶</sup>	B11 <sup>¶</sup>	B13 <sup>¶</sup>	B16 <sup>¶</sup>	B19 <sup>¶</sup>	B23 <sup>¶</sup>
1	A3 <sup>¶</sup>	A6 <sup>¶</sup>	A9 <sup>¶</sup>	A12 <sup>¶</sup>	A14 <sup>¶</sup>	A17 <sup>¶</sup>	A20 <sup>¶</sup>	A22 <sup>¶</sup>	B3 <sup>¶</sup>	B6 <sup>¶</sup>	B9 <sup>¶</sup>	B12 <sup>¶</sup>	B14 <sup>¶</sup>	B17 <sup>¶</sup>	B20 <sup>¶</sup>	B22 <sup>¶</sup>
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

Figure 2. Pin conversion top view

3.4 Pin assignment for 96-ball LFBGA

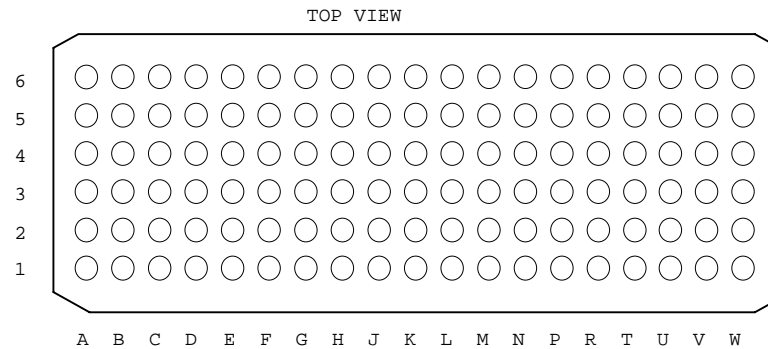
<sup>†</sup>GND: B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, and R4

<sup>‡</sup>V<sub>DD</sub>: C3, C4, F3, F4, L3, L4, P3, and P4

<sup>§</sup>Control: A3, A4, H3, H4, J3, J4, T3, and T4

<sup>¶</sup>I/O and Signals: all Row-1, -2, -5 and -6 pins.

### 3.5 114-ball LFBGA (MO-205DC)



**Figure 3. Pinout configuration**

### 3.6 3.6 Pin conversion for 114-ball LFBGA

The pin conversion adopts the naming convention of logic devices in 56-pin packages (e.g. SSOP, TSSOP, TVSOP).

6	A52 <sup>#</sup>	A49 <sup>#</sup>	A47 <sup>#</sup>	A44 <sup>#</sup>	A42 <sup>#</sup>	A40 <sup>#</sup>	A37 <sup>#</sup>	A36 <sup>#</sup>	A33 <sup>#</sup>	NC <sup>*</sup>	B52 <sup>#</sup>	B49 <sup>#</sup>	B47 <sup>#</sup>	B44 <sup>#</sup>	B42 <sup>#</sup>	B40 <sup>#</sup>	B37 <sup>#</sup>	B36 <sup>#</sup>	B33 <sup>#</sup>
5	A54 <sup>§</sup>	A51 <sup>#</sup>	A48 <sup>#</sup>	A45 <sup>#</sup>	A43 <sup>#</sup>	A41 <sup>#</sup>	A38 <sup>#</sup>	A34 <sup>#</sup>	A31 <sup>§</sup>	B55 <sup>§</sup>	B54 <sup>§</sup>	B51 <sup>#</sup>	B48 <sup>#</sup>	B45 <sup>#</sup>	B43 <sup>#</sup>	B41 <sup>#</sup>	B38 <sup>#</sup>	B34 <sup>#</sup>	B31 <sup>§</sup>
4	A55 <sup>§</sup>	A56 <sup>¶</sup>	A53 <sup>†</sup>	A50 <sup>‡</sup>	A46 <sup>†</sup>	A39 <sup>†</sup>	A35 <sup>‡</sup>	A32 <sup>†</sup>	A30 <sup>§</sup>	A29 <sup>¶</sup>	B56 <sup>¶</sup>	B53 <sup>†</sup>	B50 <sup>‡</sup>	B46 <sup>†</sup>	B39 <sup>†</sup>	B35 <sup>‡</sup>	B32 <sup>†</sup>	B30 <sup>§</sup>	B29 <sup>¶</sup>
3	A2 <sup>§</sup>	A1 <sup>§</sup>	A4 <sup>†</sup>	A7 <sup>‡</sup>	A11 <sup>†</sup>	A18 <sup>†</sup>	A22 <sup>‡</sup>	A25 <sup>†</sup>	A27 <sup>§</sup>	A28 <sup>§</sup>	B1 <sup>§</sup>	B4 <sup>†</sup>	B7 <sup>‡</sup>	B11 <sup>†</sup>	B18 <sup>†</sup>	B22 <sup>‡</sup>	B25 <sup>†</sup>	B27 <sup>§</sup>	B28 <sup>§</sup>
2	A3 <sup>§</sup>	A6 <sup>#</sup>	A9 <sup>#</sup>	A12 <sup>#</sup>	A14 <sup>#</sup>	A16 <sup>#</sup>	A19 <sup>#</sup>	A23 <sup>#</sup>	A26 <sup>§</sup>	B2 <sup>§</sup>	B3 <sup>§</sup>	B6 <sup>#</sup>	B9 <sup>#</sup>	B12 <sup>#</sup>	B14 <sup>#</sup>	B16 <sup>#</sup>	B19 <sup>#</sup>	B23 <sup>#</sup>	B26 <sup>§</sup>
1	A5 <sup>#</sup>	A8 <sup>#</sup>	A10 <sup>#</sup>	A13 <sup>#</sup>	A15 <sup>#</sup>	A17 <sup>#</sup>	A20 <sup>#</sup>	A21 <sup>#</sup>	A24 <sup>#</sup>	NC <sup>*</sup>	B5 <sup>#</sup>	B8 <sup>#</sup>	B10 <sup>#</sup>	B13 <sup>#</sup>	B15 <sup>#</sup>	B17 <sup>#</sup>	B20 <sup>#</sup>	B21 <sup>#</sup>	B24 <sup>#</sup>
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W

**Figure 4. Pin conversion top view**

<sup>†</sup>GND Pins: C3, C4, E3, E4, F3, F4, H3, H4, M3, M4, P3, P4, R3, R4, U3, and U4

<sup>‡</sup>V<sub>DD</sub> Pins: D3, D4, G3, G4, N3, N4, T3, and T4

<sup>§</sup>Control Pins: A2, A3, A4, A5, B3, J2, J3, J4, J5, K2, K3, K5, L2, L3, L5, V3, V4, W2, W3, and W5

<sup>¶</sup>GND or Control Pins: B4, K4, L4, and W4

<sup>#</sup>I/O Pins: A1, A6, B1, B2, B5, B6, C1, C2, C5, C6, D1, D2, D5, D6, E1, E2, E5, E6, F1, F2, F5, F6, G1, G2, G5, G6, H1, H2, H5, H6, J1, J6, L1, L6, M1, M2, M5, M6, N1, N2, N5, N6, P1, P2, P5, P6, R1, R2, R5, R6, T1, T2, T5, T6, U1, U2, U5, U6, V1, V2, V5, V6, W1, and W6

<sup>\*</sup>No Connection Pins: K1 and K6

## 4 Reference to other applicable JEDEC standards and publications

JEP95: JEDEC Registered and Standard Outlines for Solid State and Related Products

